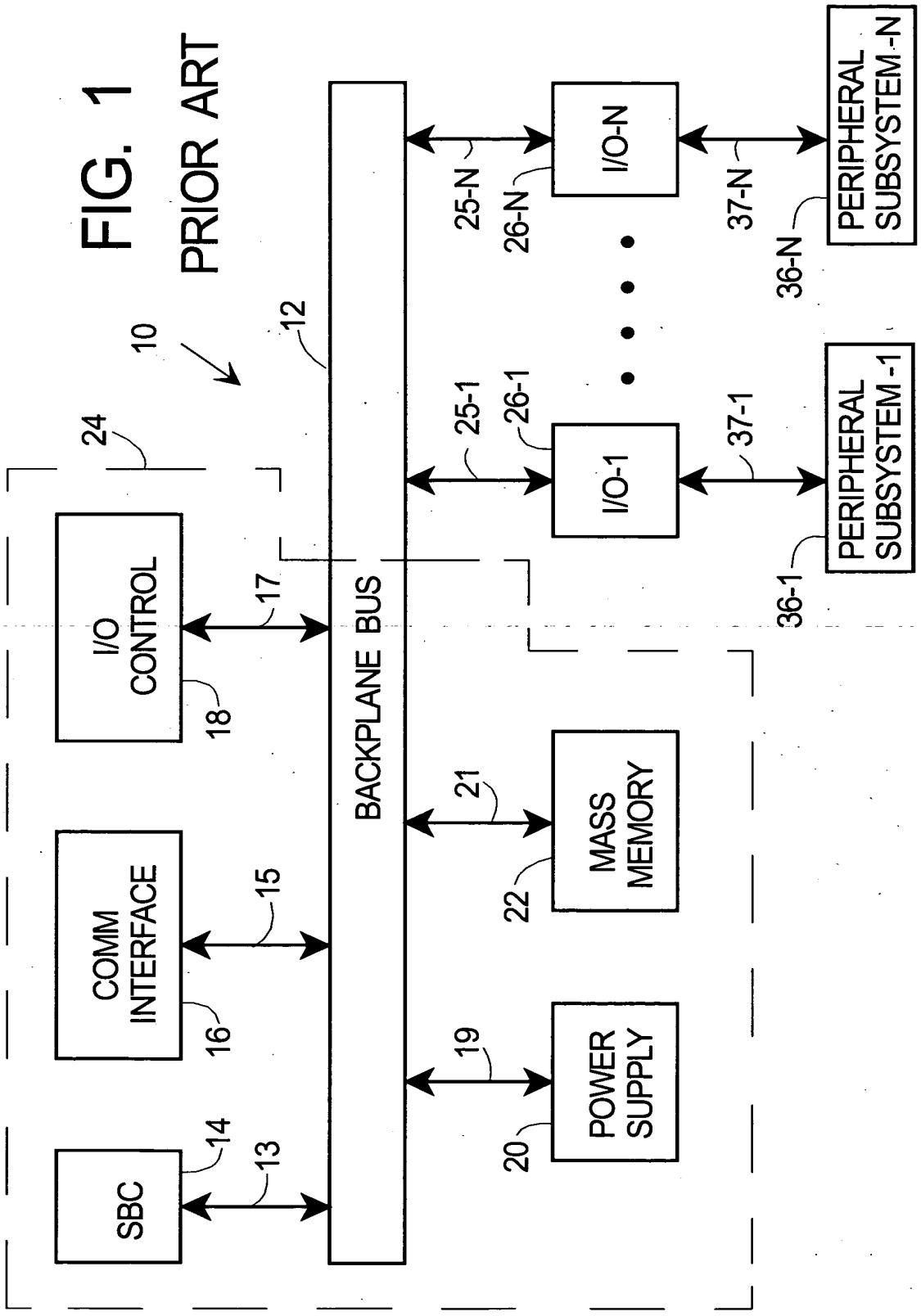
FIG. 1
PRIOR ART



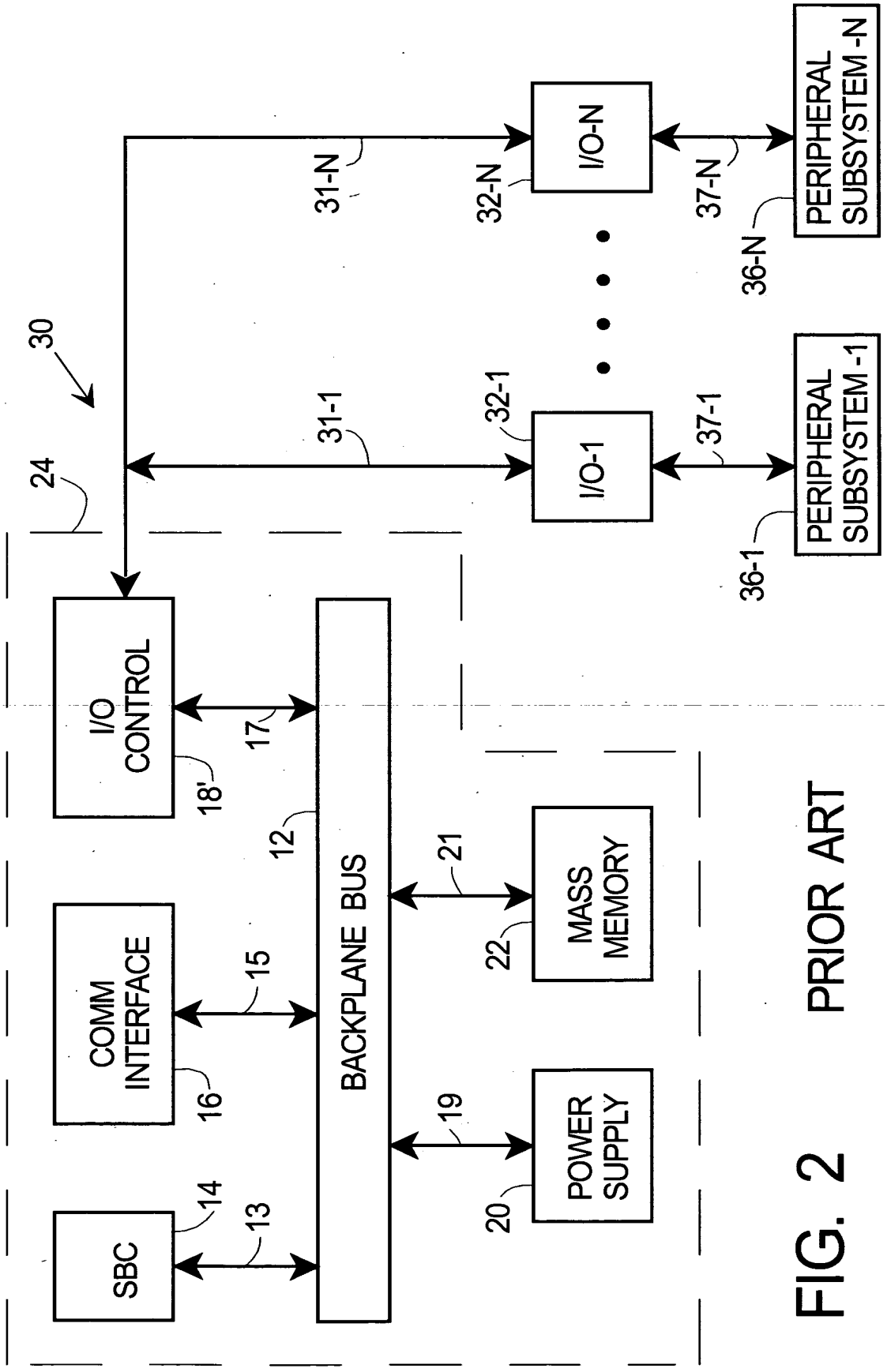


FIG. 2 PRIOR ART

FIG. 3
PRIOR ART

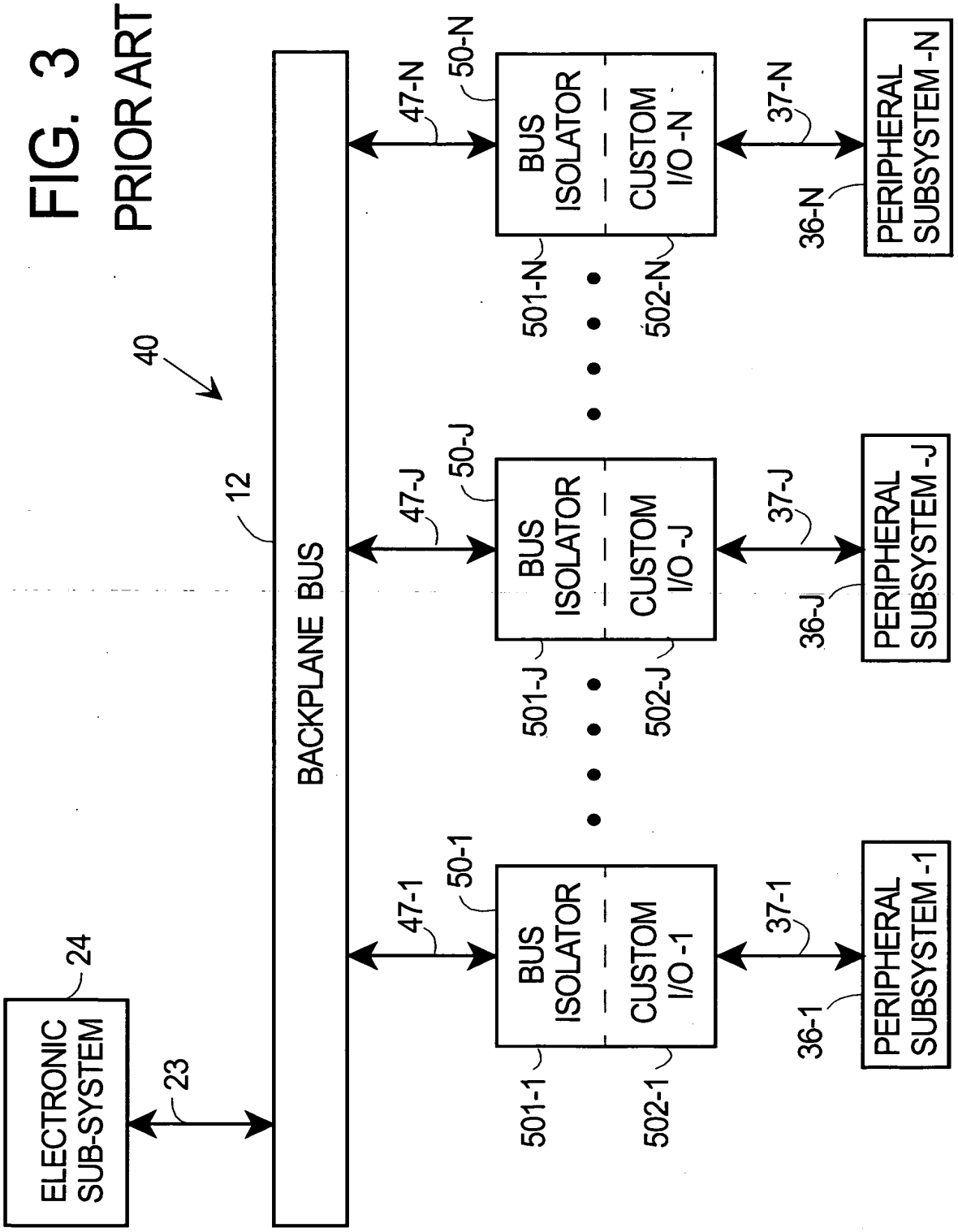
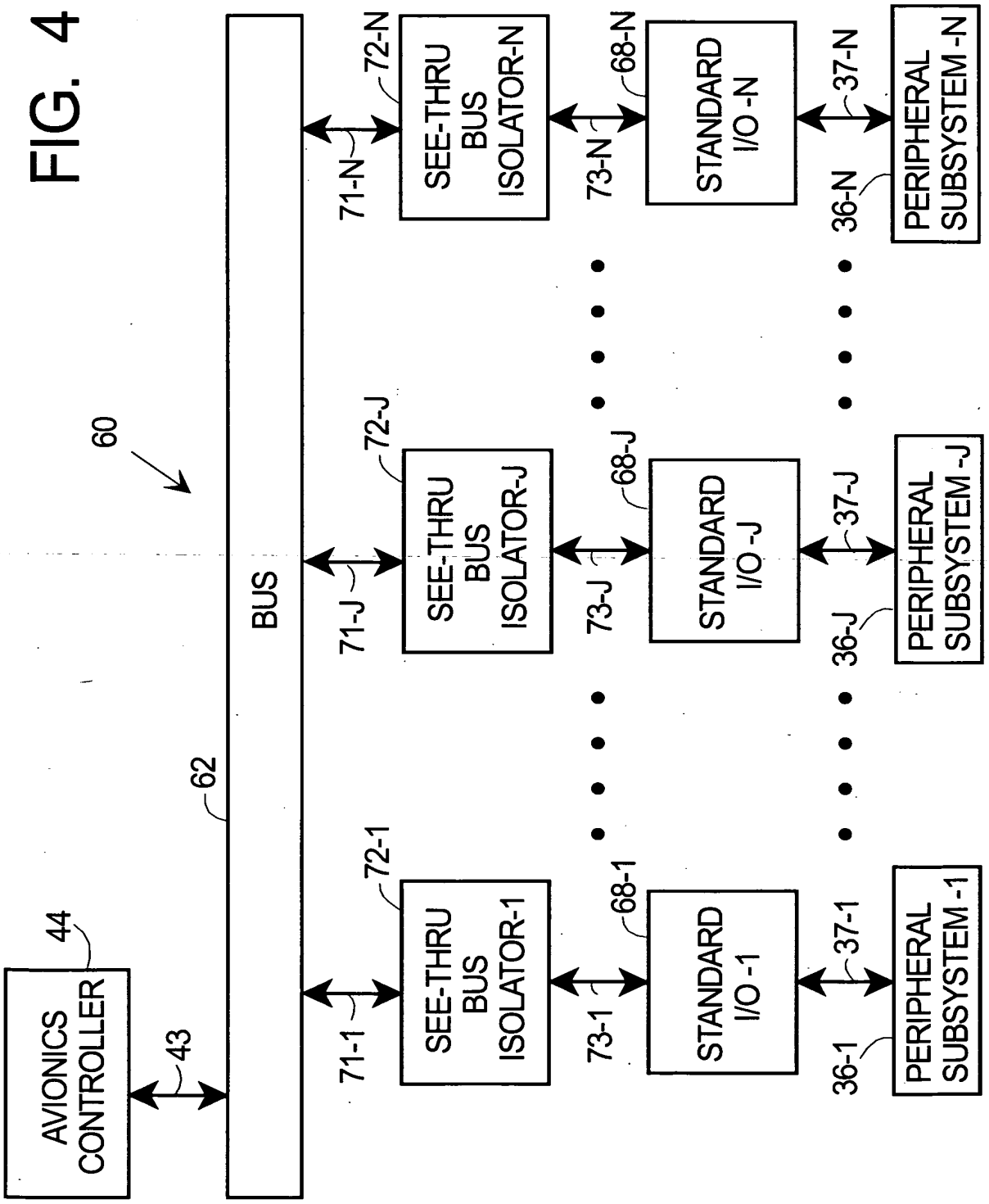


FIG. 4


60
AVIONICS CONTROLLER
44
43
62
BUS
71-1
72-1
SEE-THRU BUS ISOLATOR-1
73-1
68-1
STANDARD I/O -1
37-1
36-1
PERIPHERAL SUBSYSTEM -1
71-J
72-J
SEE-THRU BUS ISOLATOR-J
73-J
68-J
STANDARD I/O -J
37-J
36-J
PERIPHERAL SUBSYSTEM -J
71-N
72-N
SEE-THRU BUS ISOLATOR-N
73-N
68-N
STANDARD I/O -N
37-N
36-N
PERIPHERAL SUBSYSTEM -N

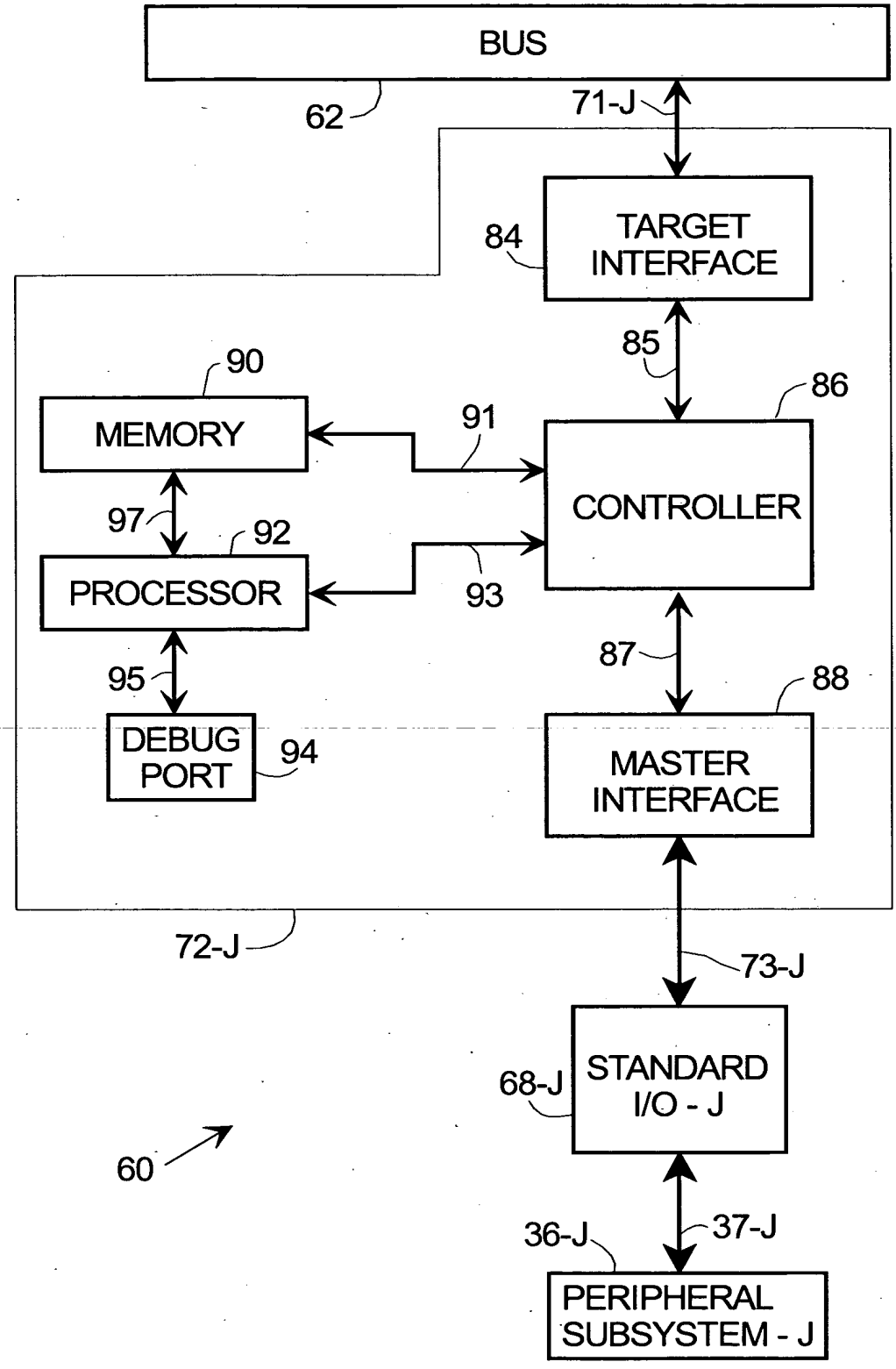

BUS
62
71-J
TARGET INTERFACE
84
85
86
90
MEMORY
91
CONTROLLER
97
92
PROCESSOR
93
87
88
95
DEBUG PORT
94
MASTER INTERFACE
72-J
73-J
STANDARD I/O - J
68-J
60
36-J
37-J
PERIPHERAL SUBSYSTEM - J

FIG. 5

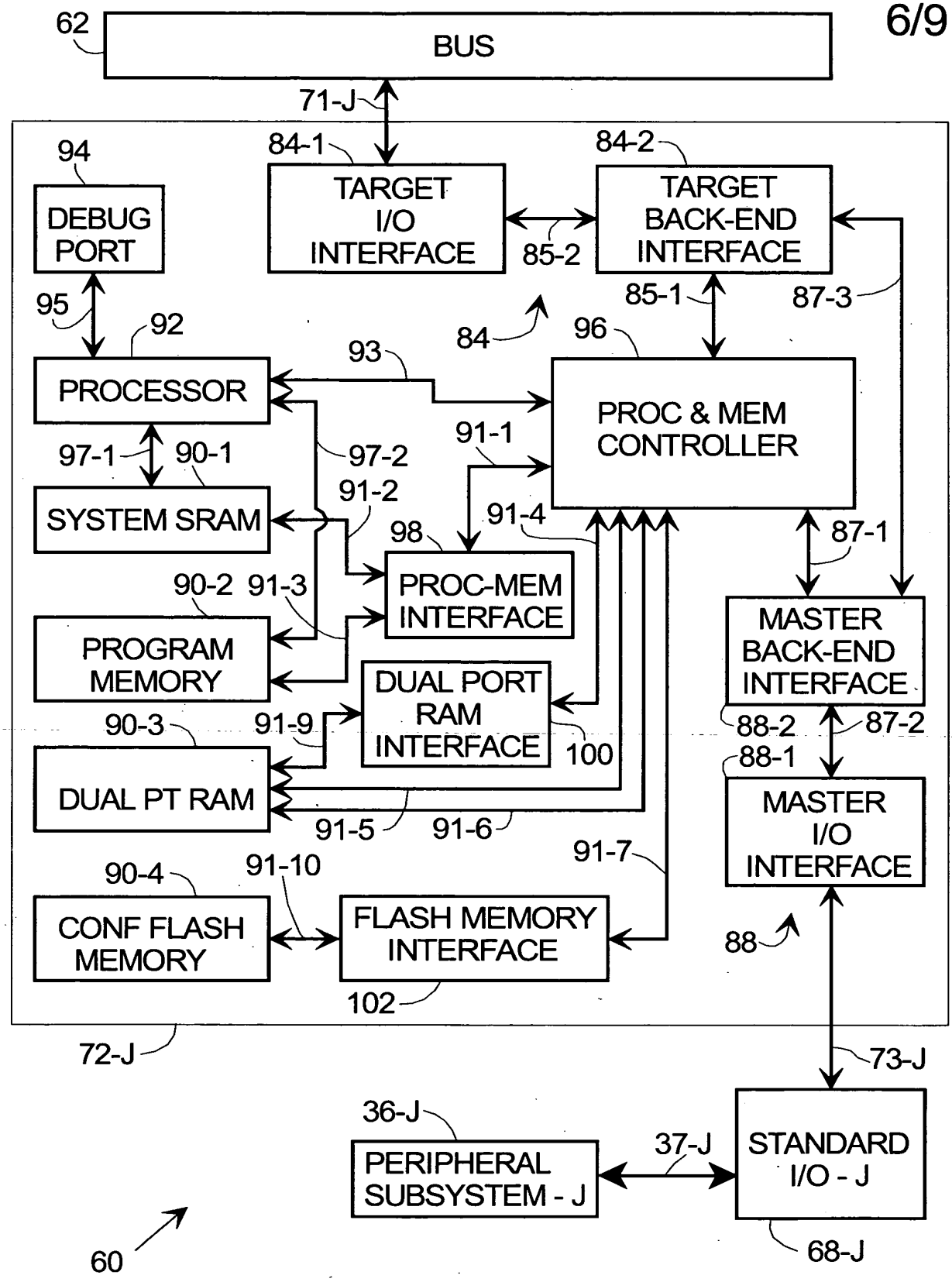

62
BUS
71-J
84-1
84-2
94
DEBUG PORT
TARGET I/O INTERFACE
85-2
TARGET BACK-END INTERFACE
85-1
87-3
95
92
84
96
93
PROCESSOR
PROC & MEM CONTROLLER
91-1
97-1
90-1
97-2
91-2
SYSTEM SRAM
91-4
98
87-1
90-2
91-3
PROC-MEM INTERFACE
MASTER BACK-END INTERFACE
PROGRAM MEMORY
DUAL PORT RAM INTERFACE
88-2
87-2
90-3
91-9
100
88-1
DUAL PT RAM
MASTER I/O INTERFACE
91-5
91-6
91-7
90-4
91-10
CONF FLASH MEMORY
FLASH MEMORY INTERFACE
88
102
72-J
73-J
36-J
37-J
STANDARD I/O - J
PERIPHERAL SUBSYSTEM - J
60
68-J

FIG. 6

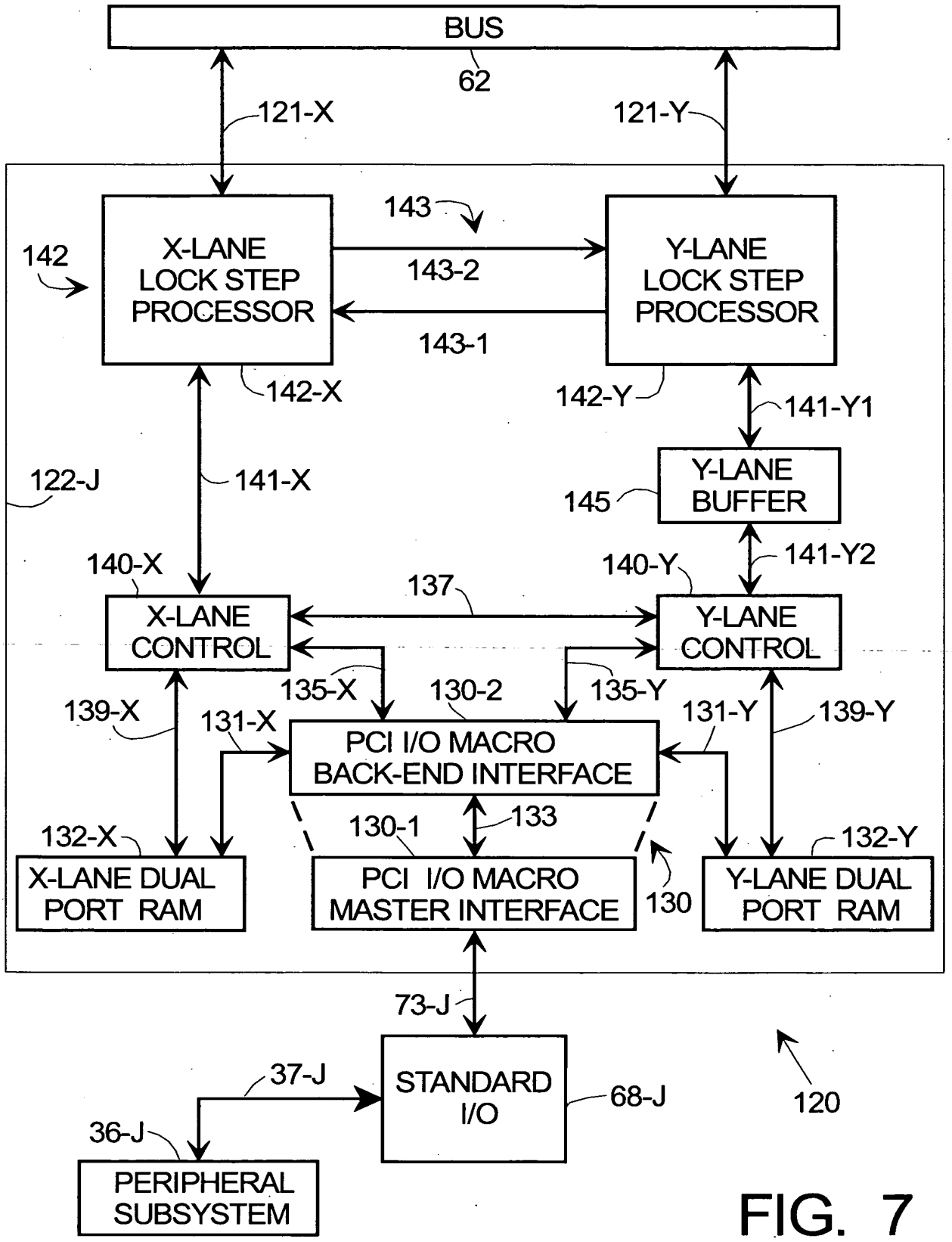

BUS
62
121-X
121-Y
143
142
X-LANE LOCK STEP PROCESSOR
143-2
143-1
Y-LANE LOCK STEP PROCESSOR
142-X
142-Y
141-Y1
122-J
141-X
Y-LANE BUFFER
145
140-X
140-Y
141-Y2
137
X-LANE CONTROL
Y-LANE CONTROL
135-X
130-2
135-Y
139-X
131-X
131-Y
139-Y
PCI I/O MACRO BACK-END INTERFACE
132-X
130-1
133
132-Y
X-LANE DUAL PORT RAM
PCI I/O MACRO MASTER INTERFACE
130
Y-LANE DUAL PORT RAM
73-J
37-J
STANDARD I/O
68-J
120
36-J
PERIPHERAL SUBSYSTEM

FIG. 7

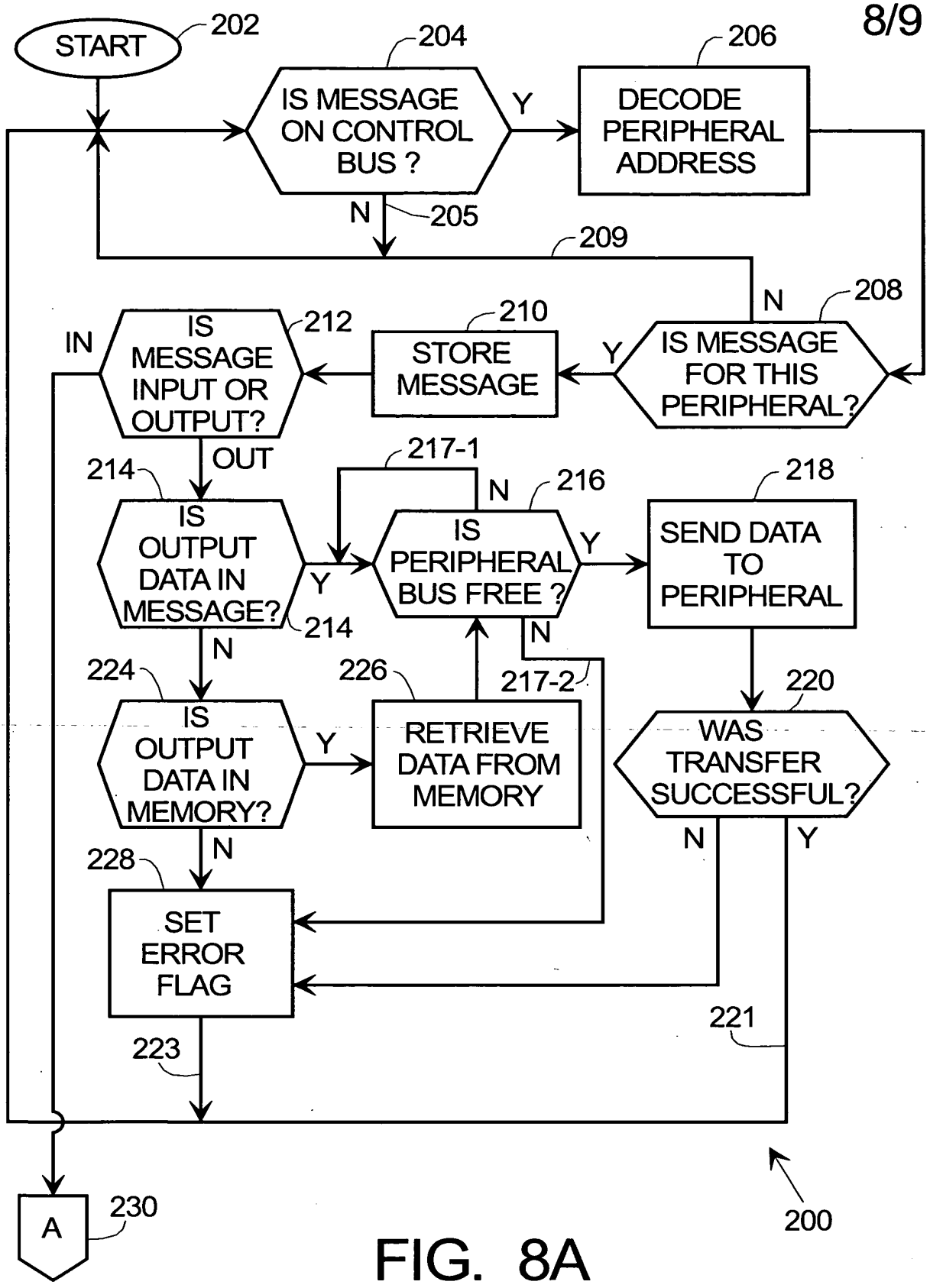

START
202
IS MESSAGE ON CONTROL BUS ?
204
Y
N
205
DECODE PERIPHERAL ADDRESS
206
209
IS MESSAGE FOR THIS PERIPHERAL?
208
N
Y
STORE MESSAGE
210
IS MESSAGE INPUT OR OUTPUT?
212
IN
OUT
IS OUTPUT DATA IN MESSAGE?
214
Y
N
214
217-1
IS PERIPHERAL BUS FREE ?
216
N
Y
SEND DATA TO PERIPHERAL
218
217-2
IS OUTPUT DATA IN MEMORY?
224
Y
N
RETRIEVE DATA FROM MEMORY
226
WAS TRANSFER SUCCESSFUL?
220
N
Y
SET ERROR FLAG
228
221
223
A
230
200

FIG. 8A

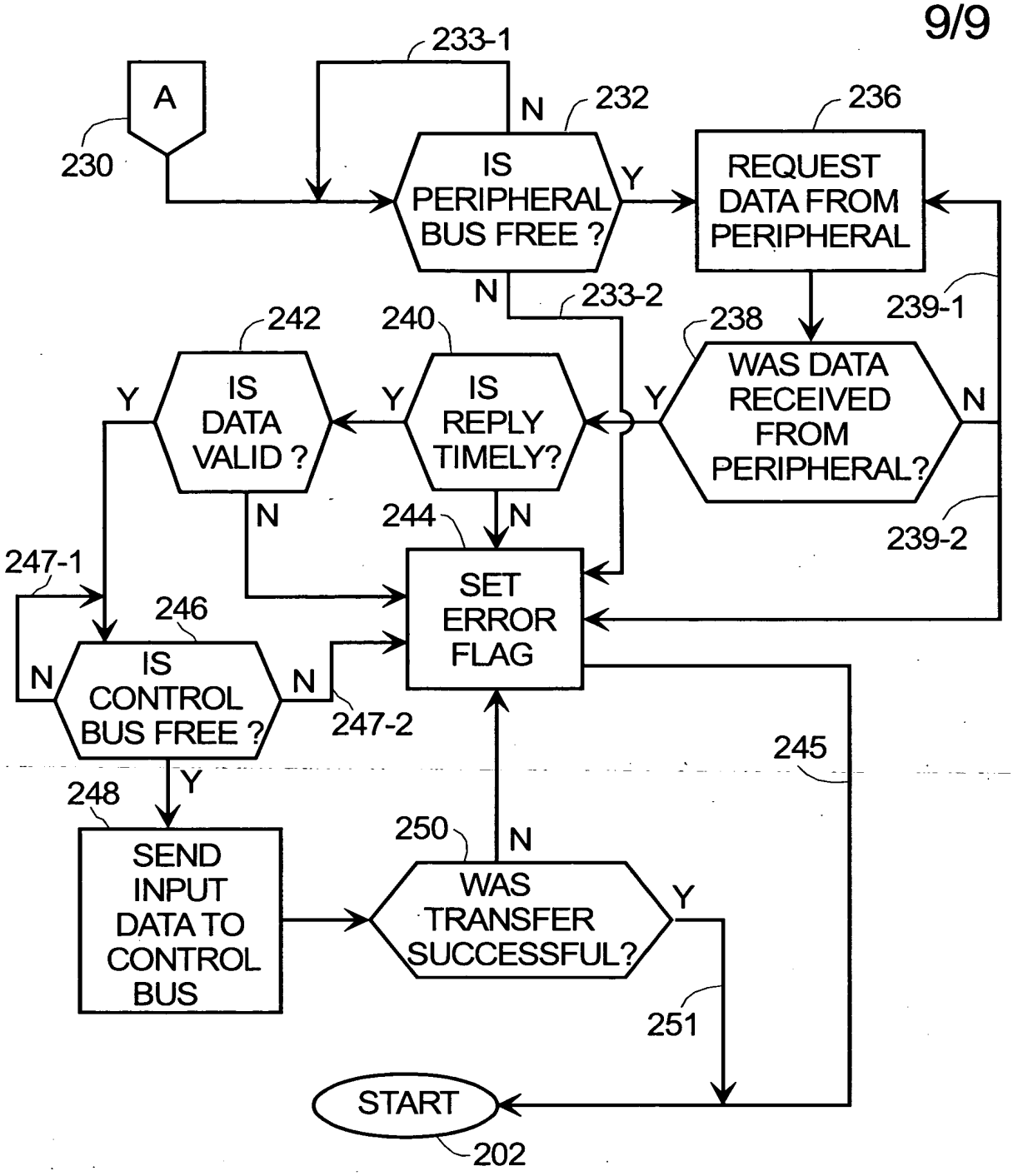

A
230
233-1
N
232
IS PERIPHERAL BUS FREE ?
Y
236
REQUEST DATA FROM PERIPHERAL
N
233-2
239-1
242
240
238
Y
IS DATA VALID ?
Y
IS REPLY TIMELY?
Y
WAS DATA RECEIVED FROM PERIPHERAL?
N
N
244
N
239-2
247-1
SET ERROR FLAG
246
N
IS CONTROL BUS FREE ?
N
247-2
245
Y
248
250
N
SEND INPUT DATA TO CONTROL BUS
WAS TRANSFER SUCCESSFUL?
Y
251
START
202

FIG. 8B

200